

**WHAT IS CLAIMED IS:**

1           1.       A method of managing power consumption in a computing system  
2       having a plurality of performance states, including a maximum performance state and  
3       a plurality of other performance states that provide successively less performance  
4       capability for an integrated circuit, the method comprising:  
5               determining utilization of the integrated circuit;  
6               comparing the determined utilization to a threshold utilization value; and  
7               if the determined utilization is above the threshold utilization value, entering a  
8               predetermined performance state as a next performance state, skipping  
9               any performance states between a current performance state and the  
10              predetermined performance state.

1           2.       The method as recited in claim 1 wherein the predetermined  
2       performance state is a maximum performance state.

1           3.       The method as recited in claim 1 wherein the predetermined  
2       performance state is a near maximum performance state.

1           4.       The method as recited in claim 1 further comprising:  
2       comparing the CPU utilization to a second threshold utilization value; and  
3       if the CPU utilization is below the second threshold utilization value, entering  
4       a next lower performance state as the next performance state.

1           5.       The method as recited in claim 1 further comprising:  
2       comparing the CPU utilization to a second threshold utilization value;  
3       if the CPU utilization is below the second threshold utilization value, entering  
4       a lower performance state as the next performance state, the lower  
5       performance state being determined according to CPU utilization.

1           6.       The method as recited in claim 4 wherein the performance state is  
2       lowered by reducing at least one of the voltage and frequency.

06676291 060701  
102090 1639490

7. The method as recited in claim 1 wherein the performance state is reduced by reducing both voltage and clock frequency of the integrated circuit.

8. The method as recited in claim 1 wherein determining the utilization is done periodically.

9. The method as recited in claim 1 wherein the integrated circuit includes a central processing unit.

10. A computing system comprising:  
an integrated circuit having multiple performance states including a maximum performance state and multiple lesser performance states;  
wherein the computing system is operable to determine utilization of the integrated circuit; and  
wherein the computing system is operable to change from a current performance state to a target performance state, skipping any performance states between the current performance state and the target performance state, in response to a determination that the utilization is above a threshold utilization value, the target performance state being the same for all performance increases.

11. The computing system as recited in claim 10 further comprising:  
a first instruction sequence operable on the integrated circuit to determine utilization of the integrated circuit; and  
a second instruction sequence operable on the integrated circuit operable to change from a current performance state to a target performance state, skipping any performance states between the current performance state and the target performance state, in response to a determination that the utilization is above a threshold utilization value, the target performance state being the same for all performance increases.

12. The computing system as recited in claim 10 wherein the target performance state is a near maximum performance state.

1

1

1

1

1

21. The computing system as recited in claim 19 further comprising:  
means for determining that the utilization is below a second threshold value  
and for always changing operation of the integrated circuit from the  
current performance state to a next lowest performance state in  
response to a determination that the utilization is below a second  
threshold utilization value.

22. The computing system as recited in claim 19 further comprising:  
means for determining that the utilization is below a second threshold value  
and for changing operation of the integrated circuit from the current  
performance state to a lower performance state in response to a  
determination that the utilization is below a second threshold  
utilization value, the lower performance state being determined  
according to the integrated circuit utilization.

23. A computer program product encoded on a computer readable medium  
comprising:  
a first instruction sequence operable on a processor having multiple  
performance states to determine utilization of the processor; and  
a second instruction sequence operable to change from a current performance  
state to a target performance state, skipping any performance states  
between the current performance state and the target performance state,  
in response to a determination that the utilization is above a threshold  
utilization value, the target performance state being the same for all  
performance increases.

24. The computer program product as recited in claim 23,  
wherein the computer readable medium is selected from the set of a disk, tape  
or other magnetic, optical, electronic storage medium, network,  
wireline, wireless or other communications medium.

1           25.     The computer program product as recited in claim 23 wherein the  
2 target performance state is one of a maximum performance state and a near maximum  
3 performance state.

1           26.     The computer program product as recited in claim 23 further  
2 comprising:  
3           a third instruction sequence operable to change operation of the processor  
4           from the current performance state to a target lower performance state  
5           in response to a determination that the utilization is below a second  
6           threshold utilization value.

1           27.     The computer program product as recited in claim 26 wherein the  
2 target lower performance state is one of a plurality of lower performance states  
3 determined according to CPU utilization.

1           28.     The computer program product as recited in claim 26 wherein the  
2 lower performance state is always a next lower performance state.